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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Manu Gulati et al.
Serial No.	10/675,745
Filed:	September 30, 2003
For:	Management of received data within host device using linked lists
Group No.:	2476
Examiner:	Ahmed, Salman

Mail Stop APPEAL
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

ARGUMENT ACCOMPANYING THE
PRE-APPEAL BRIEF REQUEST FOR REVIEW

Dear Sir:

Submitted with the Pre-Appeal Brief Request for Review are these arguments and remarks, which are being filed with the filing of a notice of appeal, accompanied by the appropriate fee, and before the filing of an appeal brief.

A final office action had been mailed December 24, 2009, advising, in sum, that Claims 1-29 in the instant patent application stand rejected as being unpatentable as obvious under 35 USC § 103(a). The rejections generally stem from a combination of Oberman and Traw, as shown below:

> Claims 1-29 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 7,042,891, to Oberman et al. ("Oberman") in view of U.S. Patent No. 5,274,768 to Traw et al. ("Traw").

1. Background

The present invention is directed towards "[e]fficient structures and processes . . . to streamline and hasten the storage and processing of incoming data so that it may be quickly routed to its intended destination." (Specification at p. 3, *ll.* 14-16).

By way of example, Applicant's Claim 1 presents a ""method for routing data *within a host device* comprising: receiving a data block at a receiver of the host device . . . *storing the data block in a receiver buffer* of the host device, wherein storing the data block in the receiver buffer *includes storing the data block in the receiver buffer at an old free linked list head address*; . . . *updating an input virtual channel linked list corresponding to the input virtual channel to include the data block*; determining an output virtual channel for the data block; *transferring the data block from the input virtual channel linked list of the receiver buffer to a destination within the host device via the output virtual channel, wherein transferring the data block from the input virtual channel linked list of the receiver buffer to a destination within the host device via the output virtual channel includes reading the data block from the receiver buffer at an old input virtual channel linked list head address*; and *updating the input virtual channel linked list to remove the data block*."

Applicant respectfully submits that a *prima facie* showing of obviousness has not been made under the hypothetical combination of the low-latency path-selection device of Oberman with ATM packet splitter of Traw.

2. low latency path-selection device of* Oberman *teaches or discloses low latency path selection and switch congestion accommodation-instead of switch congestion reduction

The low latency path-selection device of Oberman recites that to "reduce latency when the switch is not congested, the switching logic may be configured to perform a cut-though operation by routing packets directly from input ports to output ports *without storing any portion of the packet in memory*." (Oberman 2:29-33, 3:10-16, Abstract). In a congested mode, Oberman recites that "as soon as the switch becomes even slightly congested, then port interface 704A and switch fabric 140 will switch to store-and-forward routing instead of cut-through routing."

(Oberman 17:11-14). Oberman does not teach or suggest alleviating switch congestion, but to instead accommodating switch congestion.

For example, to accommodate the switch congestion and reduce packet management overhead, Oberman clusters are "used to reduce the number of bits required for tracking and managing packets. Advantageously, by dividing packets into clusters instead of cells, the overhead for each packet may potentially be reduced. For example, in one embodiment shared memory 440 may allocate memory in 128-byte clusters." (Oberman 7:42-46).

Nevertheless, the Final Office Action submits that path selection device of Oberman implicitly teaches much of that recited in Applicant's claims.

3. Final Office Action cites to the "virtual channel identifiers" of the ATM packet splitter of* Traw; *however,* Traw *teaches against the switch congestion accommodation of* Oberman *and not properly combinable

The Final Office Action, notes that the low-latency path-selection device of Oberman is silent to virtual channel technologies, because Oberman "does not explicitly [and not implicitly] teach updating an input virtual channel linked list corresponding to the input virtual channel to include the data block . . . ." (Final Office Action at p. 3).

Applicant respectfully submits that Traw does not recite data routing within a host device as set out in Applicant's claims, but instead recites use of a Reassembler 3 including a "Block 14 [that receives ATM cells from an ATM switch 7 and] splits the [ATM] cells' headers from the . . . cell bodies and passes the [Virtual Channel Identifiers (VCIs)] to the Linked List Manager 10 and the cell bodies to the Dual Port Reassembly Buffer 12. The Linked List Manager 10 creates a linked list for each VCI that identifies the locations in the Dual Port Reassembly Buffer 12 of all cell bodies associated with that VCI." (Traw 5:54-61). In turn, the linked list manager 10 "effect[s] reassembly [of the ATM cells]." (Traw 5:65).

Also, the ATM packet splitter device of Traw does not teach or suggest routing data within a host device as set out in Applicant's claims – Traw recites a SONET interface that receives an ATM packet, which splits the ATM cells' headers from the cell bodies and passes the Virtual

Channel Identifiers (VCIs) to the Linked List Manager 10 for delivery to the IBM RS/6000 Workstation 4, and not to a destination within a host device.

4. "Field of Endeavor" rationale still requires a* Graham *showing under* KSR International, *per the updated Manual of Patent Examining Procedure

For the hypothetical combination of Traw and Oberman, the Final Office Action submits that "[k]nown work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces/market place incentives if the variations are predictable to one of ordinary skill in the art." (Final Office Action at pp. 5, 10, 18, 22, 27, 31, 35; referring to Traw as "in the same or similar field of endeavor . . . (columns 5-6, lines 65-11 . . . .)(*see*, e.g., Final Office Action at p. 3)). As understood, the Final Office Action supports its "field of endeavor" consideration by referring to the foot-pedal sensor-position case of *KSR International v. Teleflex, Inc.*, 550 U.S. 398 (2007) (decided April 30, 2007); *see* Final Office Action at pp. 40-41.

For a "field of endeavor" rationale, the foot-pedal sensor-position case of *KSR International* still requires a showing of the *Graham* factors for a rejection under Section 103, and the updated Manual of Patent Examining Procedure echoes the need for this showing. (*see* MPEP 2143 at page 2100-136 (Rev. 6, Sept. 2007)(Office personnel must resolve/articulate the *Graham* factual inquiries)). Applicant respectfully submits that such findings under the MPEP or *Graham* have not been presented for the basis of rejection.

5. Applicant respectfully submits that an inventor would not turn to the low latency path selection device of Oberman with the ATM packet splitter device of Traw to achieve Applicant's invention as set out in its claims

Corollaries of Oberman and Traw are pointed to in the Final Office Action without a showing that a skilled artisan, confronted with the same problems as the inventor and with no knowledge of Applicant's claims, would select elements from the low latency path selection of Oberman and the ATM packet splitter of Traw to achieve the invention of Applicant's claims.

To avoid improper reconstruction based upon an Applicant's disclosure, the Federal Circuit submits that "the examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the

elements from the cited prior art references for combination in the manner claimed." *In re Rouffet*, 149 F.3d 1350, 1356 (Fed. Cir. 1998) (citations omitted); *In re Translogic Technology, Inc.*, 504 F.3d 1249 (Fed Cir. 2007) (post-*KSR* opinion citing *In re Rouffet* with approval); *see also* Final Office Action at pp. 38-39 (citing *In re Keller*, 642 F.2d 413 (CCPA 1981)) ("test [for obviousness] is what the combined teachings of the references would have suggested to those of ordinary skill in the art.").

As a result, Applicant respectfully submits that because of the disparate teachings of the cited references, a skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention would not turn to the low latency path selection device of Oberman and the ATM packet splitter of Traw.

6. Conclusion

Applicant respectfully submits a *prima facie* showing of obviousness has not been presented. Under the guidance of *In re Rouffet*, there is no suggestion or motivation for the hypothetical combination of the low-latency path-selection of Oberman with the dissimilar ATM cell splitter of Traw. Further, Applicant respectfully submits that the necessary findings to provide a "field of endeavor" determination has not been presented.

Also, the corollaries pulled from the low-latency path-selection device of Oberman and the ATM cell splitter of Traw do not teach or suggest all of Applicant's claim limitations. For example, these cited references do not refer to transferring data blocks from an input virtual channel linked list of a receiver buffer to a destination within the host device via an output virtual channel.

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